REMARKS

Claims 20-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over the applicant's prior art figure (APAF) is view of Yamazaki et al. (US 6,677,613 B1). Response to the Office Action identified above is listed below.

1. Rejection of Claims 20-28 under 35 U.S.C. 112:

Claims 20-28 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skill in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claim 20 discloses the limitation of "the source/drain being in the active area not covered by the gate." The applicant's drawings (fig.11) show that the gate layer (214) is formed above the source drain regions (215/216). The specification also does not disclose that the active area is not covered by the gate.

Response:

Claim 20 is amended in the above **AMENDMENTS TO THE CLAIMS** section. Fig.8 is amended and Fig.15 is added in the above **AMENDMENTS TO THE DRAWINGS** section and paragraphs [0023], [0026], [0029] are amended in the **AMENDMENTS TO THE SPECIFICATION** section. In Fig.11, the gate layer (214) is above the source/drain regions (215/216) because this cross-sectional diagram is drawn along A-A' in Fig.8. Actually, either of the source region 215 and the drain region 216 is in the

front or in the back of the gate layer 214.

Fig.15 is drawn along line B-B' in Fig.8 such that at least one complete transistor 106 is shown in a cross section so as to illustrate the relative sites for sources 215, drains 216, and gates 214 more clearly. In Fig.15, it is very obviously that the source 215 and the drain 216 are in the active area 104 not covered by the gate 214. No new matter is added. Reconsideration of the rejection over claims 20-28 is hereby requested.

2. Rejection of Claims 20-28 under 35 U.S.C. 103(a):

Claims 20-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over the applicant's prior art figure (APAF) in view of Yamazaki et al. (US 6,677,613 B1).

In re claim 20, the APAF 7 shows a microdisplay pixel cell device comprising a semiconductor substrate defined with a plurality of active areas at least one gate (52), the gate covering a portion of the active area, at least one source/drains (63/64), the source/drain being in the active area, and a first dielectric layer (66) the first dielectric layer covering the gate and the source/drain. The first dielectric layer comprises at least one row select contact plug (68) to electrically connect to the gate and at least one row select line, the row select line being atop the first dielectric layer, the row select line being electrically connected to the gate through the row select contact plug. There is at least one pixel cap top plate (42) on the first dielectric layer, at least one capacitor dielectric layer (45), the capacitor dielectric layer being atop the surface of the top plate; and at least one pixel cap bottom plate (54). The

APAF 7 shows all of the elements of the claims except the second dielectric layer being atop the first dielectric layer. Yamazaki et al. shows (figs. 1A-3) a pixel cell device comprising a first dielectric layer (125) formed over a gate (109), and a second dielectric layer (134) formed on the first dielectric layer. Yamazaki also shows a pixel cap bottom plate (139) being atop the second dielectric layer and covering a capacitor top plate (135) and a capacitor dielectric layer (135). With the capacitor being formed simultaneously being formed with the light shielding layer, the area of the pixel electrode could be reduced and a sufficient capacitance could be provided (col.9, lines 29-35).

In re claim 21, the APAF 7 shows that the gate comprises a gate oxide layer (44), a polysilicon layer or a metal silicide layer.

In re claim 22, Yamazaki et al. shows (fig.3) at least one first contact plug is comprised in the first dielectric layer and the second dielectric layer for electrically connecting the source (146) and the top plate.

In re claim 23, Yamazaki et al. shows (fig.3) at least one second contact plug (145) is comprised in the first dielectric layer and the second dielectric layer for electrically connecting the drain to the video data line.

In re claim 24, the APAF 7 discloses (pg. 4, para. [0014]) that the row select line is composed of a metal and is used as a scan line of the microdisplay.

In re claim 25, the APAF 7 discloses (pg. 4, para [0016]) that both the bottom plate and the top plate are composed of a metal.

Response:

First, the Applicant intends to point out the difference between the amended claim 20 of the present application and Yamazaki's disclosure. The amended claim 20 of the present application is repeated below:

20. (Currently amended) A microdisplay pixel cell device, the device comprising:

a semiconductor substrate defined with a plurality of active areas;

at least one gate, the gate covering a portion of the active area;

at least one source and at least one drain, the source and the drain being in the active area not covered by the gate;

a first dielectric layer, the first dielectric layer covering the gate and the source and the drain, the first dielectric layer comprising at least one row select contact plug to electrically connect to the gate;

at least one row select line, the row select line being atop the first dielectric layer, the row select line being electrically connected to the gate through the row select contact plug;

a second dielectric layer, the second dielectric layer being atop the first dielectric layer and covering the row select line;

at least one pixel cap top plate, the pixel cap top plate being atop the second dielectric layer;

at least one first contact plug, the first contact plug being in the first dielectric layer and the second dielectric layer for electrically connecting the

source and the top plate;

at least one capacitor dielectric layer, the capacitor dielectric layer being atop the surface of the top plate; and

at least one pixel cap bottom plate, the pixel cap bottom plate being atop the second dielectric layer and covering the top plate and the capacitor dielectric layer.

As disclosed in the amended claim 20 and paragraph [0036] of the present application, there are two obvious differences between Yamazaki's disclosure and the present application. In the present application, each of the sources 215 is electrically connected to the top plate 228 (the pixel cap top plate 110 in Fig.8) through each of the source contact plugs b' in the second dielectric layer 226 and the first dielectric layer 218. In addition, each of the drains 216 is electrically connected to the video data line through each of the plurality of drain contact plugs a' in the second dielectric layer 226 and the first dielectric layer 218.

According to Yamazaki's disclosure, the drain 146 is electrically connected to the electrode 139, which is also a pixel electrode, through a drain wiring 132 at a contact hole 147 through openings 137, 138. In addition, the source 145 is electrically connected to the signal line driver 703 through a source wiring 131 (also refer to col.13, lines 7-27 and Fig.7). Therefore, Yamazaki has never taught the same structure as the present application structure.

From the above discussion, the Applicant believes that the amended claim 20 of the present application is absolutely different from the combination of the applicant's prior art figure and Yamazaki's disclusure. Reconsideration of the rejection over claim 20 is hereby requested.

As claims 21, and 23-28 are dependent upon claim 20, they should be allowed if claim 20 is allowed. Reconsideration of the rejection over claim 21 and 23-28 is therefore requested.

Sincerely yours,

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AMENDMENTS TO THE DRAWINGS

The attached sheets of drawing include changes to Fig. 8 and a new added sheet of Fig.15. The sheet, which includes Fig. 7-8, replaces the original sheet including Fig. 7-8. In Figure 8, a cross-sectional line B-B' previously omitted has been added and the arrows for indicating two source contact plugs b' are shifted. Fig.15, which is a cross-sectional diagram along line B-B' in Fig.8, has been added in order to illustrate the sites for sources, drains, and gates, which has already been shown in Fig.8, more clearly.

Attachment: Replacement Sheet
Annotated Sheet Showing Changes

Attachments

Replacement Sheet

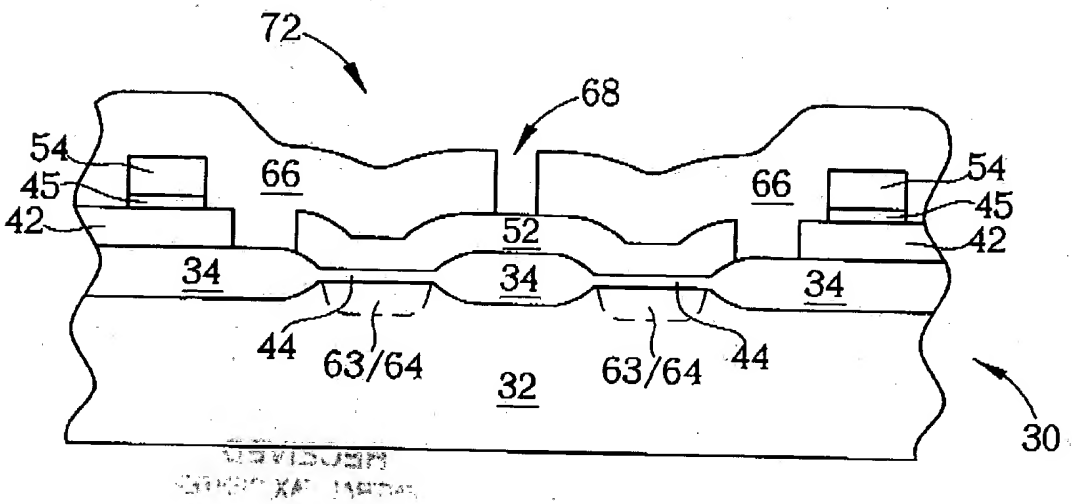

Fig. 7 Prior art

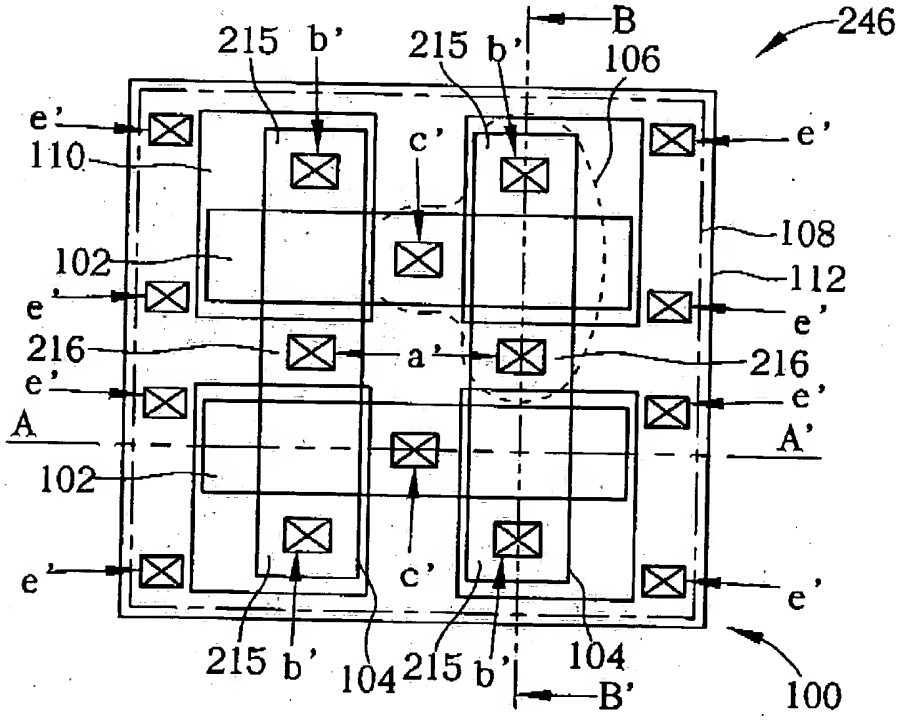

Fig. 8

Annotated Sheet Showing Changes

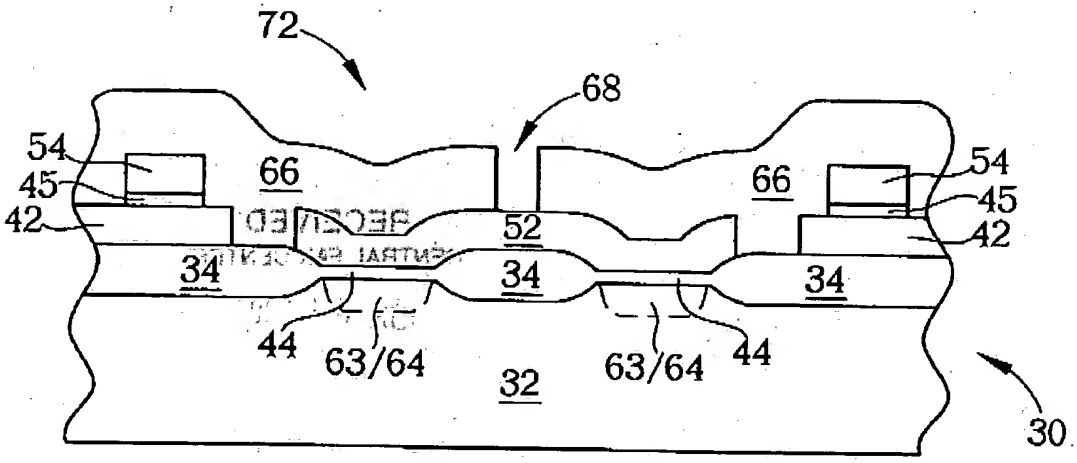

Fig. 7 Prior art

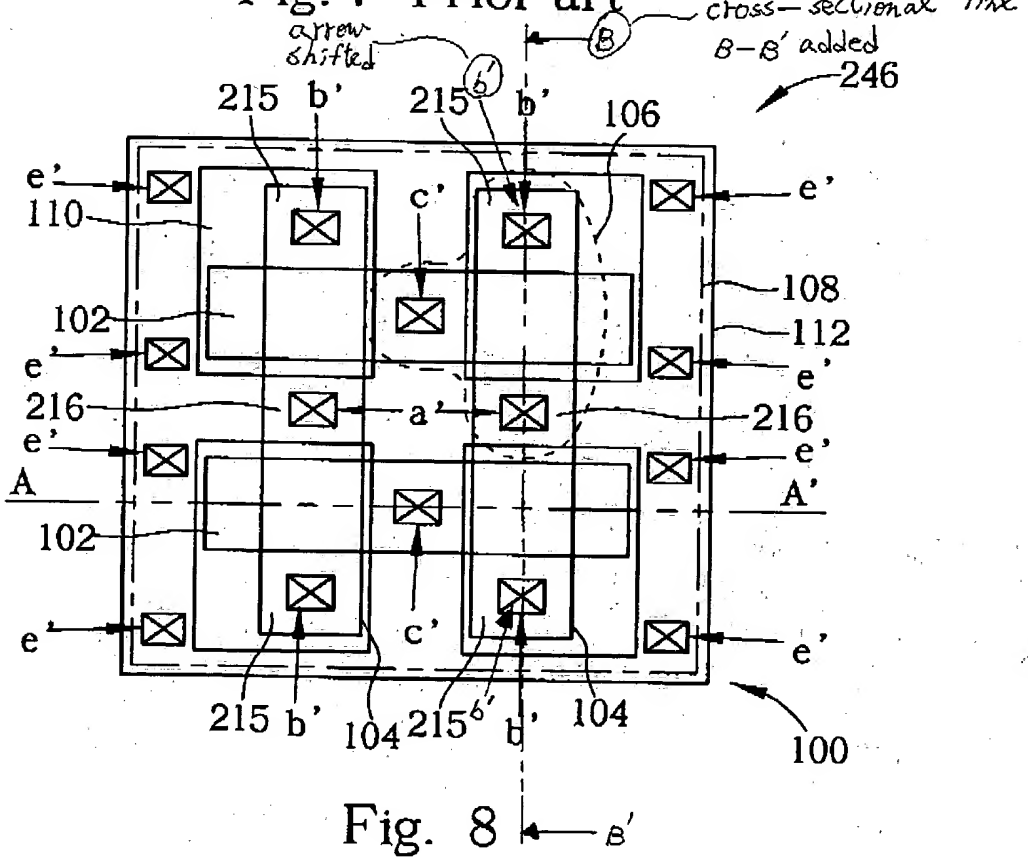

Fig. 8 B'

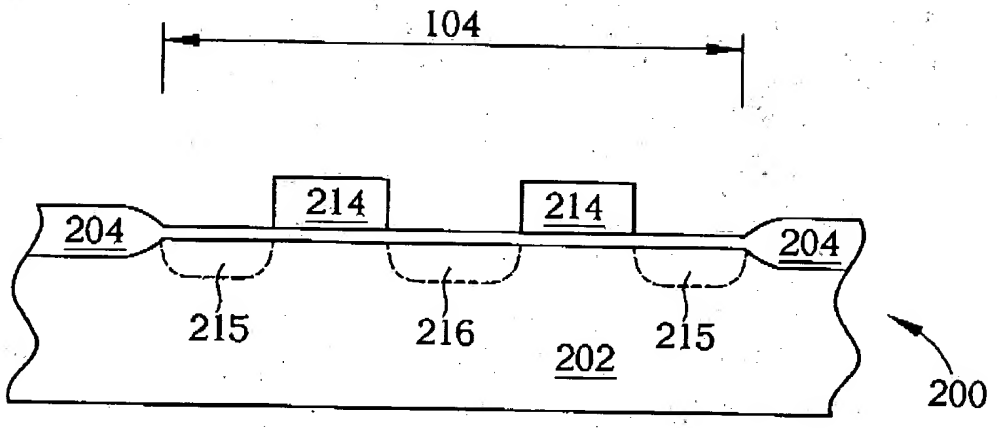

Fig. 15